PI3EQXDP1201

3.3V, 4-Ch DisplayPort 1.2 Redriver with Aux Listener/AutoTest mode

Features

- Compliant with VESA DisplayPort 1.2 specification for HBR2, HBR, RBR rate (5.4/2.7/1.62Gbps)
- Dual mode DisplayPort Outputs by providing DDC signals across the Aux sink pin
- Built-in Aux interception circuit only listen to the link training, but does not affect link training
- Sink Request Auto Test Mode through Aux Channels
- Dynamic EQ through Aux configuration register programming for deterministic jitter reduction
- Cable Detection pins, toggle between DP and TMDS mode
- Automatic power down state when HPD signal is low
- Low insertion loss across the Aux signal path
- Dedicated pin control mode for Equalization setting control
- Internally Biased AC coupled in Aux channel
- Single Power Supply: 3.3V
- Integrated ESD protection
- Package : 48-pin TQFN, 7mm x 7mm

Description

PI3EQXDP1201 provides the ability to reduce signal jitter by transmission line effects to enable longer cable length on the 5.4Gbps DisplayPort1.2 signals.

Integrated AUX decoder can support Displayport link training. It can decipher the link training message and automatically configure Displayport differential signal outputs with the best pre-emphasis and output swing level settings.

Input Equalization, Output level swing and pre-emphasis are controlled by either Aux link snooping or pin configuration. Decoding of the Aux command happens during link training.

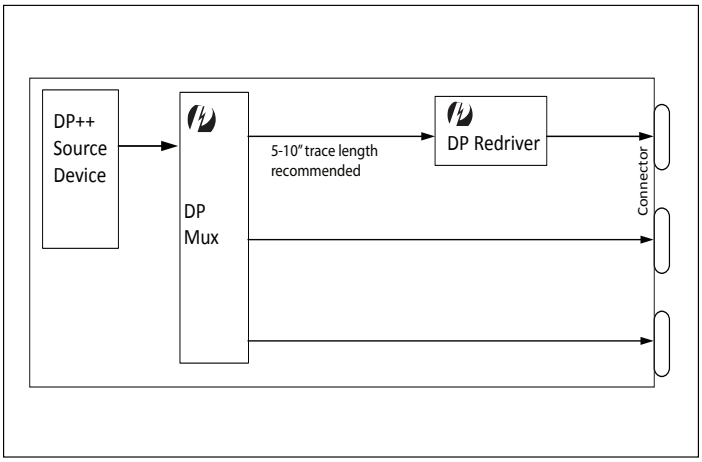
Built-in Sync Request Auto Test mode enables users to complete DisplayPort link status through Aux channels in minutes.

PI3EQXDP1201 is intended for use in any systems, DP signal compliance is required, including notebook PC and docking stations, Graphic cards and digital video systems.

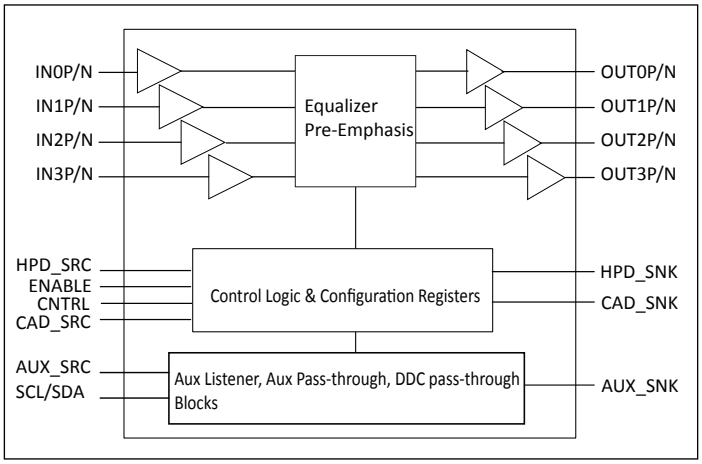
Applications

- Notebook and Dock station
- PC system boards
- Digital video systems

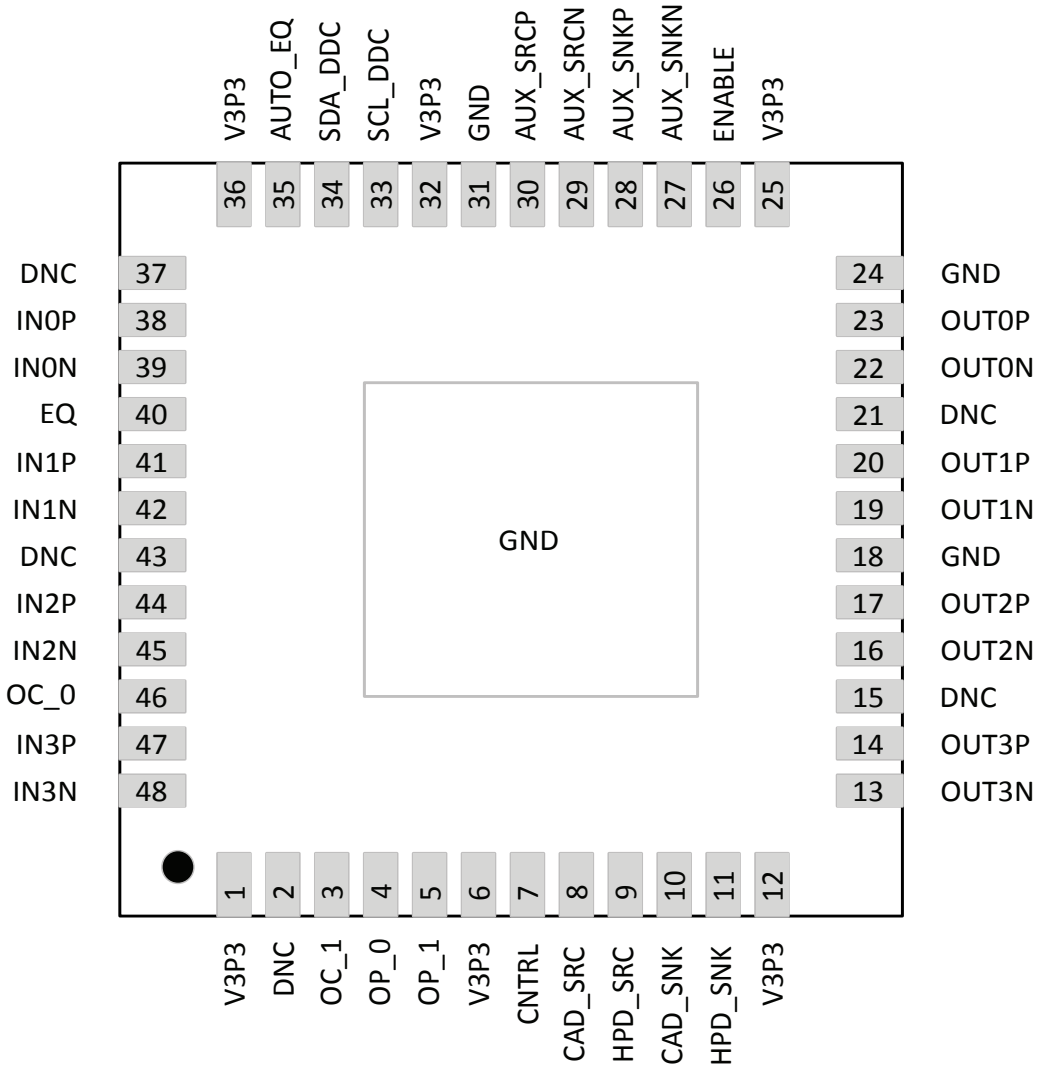
Typical Application



Functional Block Diagram



Package Pinout



Pin Description

Pin #	Pin Name	Pin Type	Description
1	V3P3	Power	3.3V +/10% Power rail
2	DNC	NC	Do Not Connect; leave pin floating
3	OC_1	Input	Swing control bit 1. Pulled-up internally with 100kOhm See truth tables for functionality
4	OP_0	Input	Pre-emphasis control bit 1. Internally pulled-up with 100kOhm See truth tables for functionality
5	OP_1	Input	Pre-emphasis control bit 0. Internally pulled-up with 100kOhm See truth tables for functionality
6	V3P3	Power	3.3V +/-10% Power rail
7	CNTRL	Input	Configure Output Voltage Swing and Pre-Emphasis (See truth table for functionality)
8	CAD_SRC	Output	Cable Adapter Detection from DP connector CAD_SRC = "0" : no cable adapter; enable DP ReDriver mode with AUX listening and link training active CAD_SRC = "1" & Installed cable adapter; enable TMDS ReDriver mode and disable AUX interception
9	HPD_SRC	Output	Hot Plug detect to system DP source. 3.3V CMOS output.
10	CAD_SNK	Input	Cable detect from sink side.
11	HPD_SNK	Input	Hot Plug Detect from the sink side 200kOhm Pull-down
12	V3P3	Power	3.3V +/- 10% Power rail
13	OUT3N	Output	Lane 3 data negative output
14	OUT3P	Output	Lane 3 data positive output
15	DNC	NC	Do Not Connect
16	OUT2N	Output	Lane 2 data negative output
17	OUT2P	Output	Lane 2 data positive output
18	GND	Power	Ground
19	OUT1N	Output	Lane 1 data negative output
20	OUT1P	Output	Lane 1 data positive output
21	DNC	NC	Do Not Connect
22	OUT0N	Output	Lane 0 data negative output
23	OUT0P	Output	Lane 0 data positive output
24	GND	Power	Ground
25	V3P3	Power	3.3V +/10% Power rail
26	ENABLE	Input	External Power Down pin "1"=Enable ; "0"=Disable ; Pulled-up internally with 100kOhm
27	AUX_SNKN	I/O	AUX negative channel connected to DP sink device
28	AUX_SNKP	I/O	AUX positive channel connected to DP sink device

continued >

Pin Description

Pin #	Pin Name	Pin Type	Description
29	AUX_SRCN	I/O	AUX negative channel connected to DP source device
30	AUX_SRCP	I/O	AUX positive channel connected to DP source device
31	GND	Power	Ground
32	V3P3	Power	3.3V +/10% Power rail
33	SCL_DDC	I/O	DDC clock channel from source side when CAD_SNK=1
34	SDA_DDC	I/O	DDC Data channel from source side when CAD_SNK=1
35	AUTO_EQ	Input	Auto EQ Control pin. Enable = "1", Disable = "0". This pin is internally pulled up through 100kOhm. EQ-pin (Pin 40) can control Auto EQ mode 0, 1 and 2.
36	V3P3	Power	3.3V +/10% Power rail
37	DNC	NC	Do Not Connect
38	IN0P	Input	Lane 0 data positive input
39	IN0N	Input	Lane 0 data negative input
40	EQ	Input	Be able to configure Fixed EQ setting, when disable Auto-EQ mode (AUTO_EQ pin ="0"). This pin is internally biased to 50% of V3P3.
41	IN1P	Input	Lane 1 data positive input
42	IN1N	Input	Lane 1 data negative input
43	DNC	NC	Do Not Connect
44	IN2P	Input	Lane 2 data positive input
45	IN2N	Input	Lane 2 data negative input
46	OC_0	Input	Output Control pin. See Output Control truth table for functionality Internally pulled-high with 100kOhm
47	IN3P	Input	Lane 3 data positive input
48	IN3N	Input	Lane 3 data negative input

Control Pin Functional Tables

Mode	Control Pins				Output Swing	Pre-emphasis	EQ setting
	CNTRL	CAD SINK	OC_1, OC_0	OP_1, OP_0			
Normal Mode	0	1	X X	X X	800mV	0dB	Follow Auto EQ & Fixed EQ Table
	0	0	X, X	X,X	Follow listener	Follow listener	Follow Auto EQ & Fixed EQ Table
Test Mode	1	X	0 0	1 1	400mV	0dB`	Pin Control
	1	X	0 0	0 0	400mV	3.5dB	Pin Control
	1	X	0 0	0 1	400mV	6dB	Pin Control
	1	X	0 0	1 0	400mV	9.5dB	Pin Control
	1	X	0 1	1 1	600mV	0dB	Pin Control
	1	X	0 1	0 0	600mV	3.5dB	Pin Control
	1	X	0 1	0 1 / 1 0	600mV	6dB	Pin Control
	1	X	1 1	1 1	800mV	0dB	Pin Control
	1	X	1 1	0 X / 1 0	800mV	3.5dB	Pin Control
	1	X	1 0	XX	1200mV	0dB	Pin Control

Normal Mode

Normal Mode	Auto EQ mode 0	Auto EQ mode 1	Auto EQ mode 2	Fixed Eq. 2.5dB @ 2.7GHz	Fixed Eq. 5.1dB @ 2.7GHz	Fixed Eq. 7.2dB @ 2.7GHz	Notes
EQ	L	M	H	L	M	H	EQ pin is internally biased to ~50% of V3P3 at "M(Middle)" or floating statue. **Measured Gains**
Auto EQ	H	H	H	L	L	L	Auto EQ pin has a internal pull-up.

	1.62G	**2.7G**	**5.4G**	Unit
L	-1.42	-2.01	-2.79	dB
M	2.41	3.9	5.16	dB
H	6.96	9.28	10.8	dB

EQ Setting in Auto EQ Mode

PRE-EMPHASIS_SET Bit[4:3] in DPCD registers	**Auto EQ mode 0**			**Auto EQ mode 1**			**Auto EQ mode 2**			Unit
	1.62G	**2.7G**	**5.4G**	**1.62G**	**2.7G**	**5.4G**	**1.62G**	**2.7G**	**5.4G**	
0 0	2.26	2.74	2.49	3.97	5.92	7.3	3.97	7.27	8.69	dB
0 1	0.34	0.57	0.22	1.44	2.5	3.41	3.21	5.1	6.42	dB
1 0	-1.42	-2.01	-2.79	0.34	0.57	0.22	1.44	2.5	3.41	dB
1 1	-2.39	-3.62	-4.71	-1.42	-2.01	-2.79	0.34	0.57	0.22	dB

Functional Description

Intelligent Power Management

Pericom's block based design and intelligent detection scheme allow portions, or all of the IC, to be disabled for power savings. For example, in DP mode, if only one or two lanes are active, the other lanes will be automatically powered off. If there is no input video signal the entire IC will be powered down. If there is no monitor detected, Pericom's PI3EQXDP1201 can also automatically power down the IC. This intelligent power management concept not only saves system power, but also stops the device from outputting useless data or noise when no signal is present at the input of the IC. The power-down mode can also be entered using hard pin ENABLE, or through DPCD register (AUX link training)

DisplayPort AUX Listener

PI3EQXDP1201 integrates an AUX listener(decoder), which enables the device to receive and decipher all AUX link training data and use this extracted information for its own configuration. The intercepted DPCD data is used to adjust the active lane count, output swing level, output pre-emphasis level, and to manage the device's D3 power saving state.

AUX Listener Specification

DP AUX listener will support Native AUX CH Syntax. *Mapping of I^2C onto AUX CH Syntax is not supported.* AUX listener monitors AUX channel from requester and replier for transactions and stored AUX command from requester and reply command from sinks that are related to the link settings. AUX listener recovered the clock from AUX data input by cycle counting the synchronization pulse at the beginning of the AUX cycle. In a AUX write request cycle, the AUX address compare the addresses with the following registers' address, data is extracted and stored into the respective registers when the addresses matches. These registers are set during link training sequence following hot plug detection.

00100h	Data Rate Register
00101h	LANE_COUNT_SET
00103h	TRAINING_LANE0_SET
00104h	TRAINING_LANE1_SET
00105h	TRAINING_LANE2_SET
00106h	TRAINING_LANE3_SET
00260h	Sink Test request response
00600h	Power Down

The AUX listener support Sink request Test sequence. After HPD IRQ event and DP source read 00201h AUX register and if bit 1 is high, the DP source will enter a Sink request test mode and initiate a sequence of AUX read request cycle. During the read cycle, data matching the following registers address are stored in the listener.

00206h	ADJUST_REQUEST_LANE0_1
00207h	ADJUST_REQUEST_LANE2_3
00218h	Test Request
00219h	Test link rate
00220h	Test Lane count

After the read request cycle, the DP source will write 1 to Bit 0 register 00260h if the DP source enters sink request mode, or 1 to Bit 1 of register 00260h if the source declined the sink test request. The data stored in registers 002xx above will override the value set in 00101h to 00106h registers when the sink entered the Sink Test mode.

Sink Test Request Acknowledgement

00260h	mode	Buffer configuration outputs
xxxxxx00b	No action	00100 : 00106h
xxxxxx01b	Sink Test mode	00206h,00207h,00219h,00220h Override 00100,1,3,4,5,6h register settings
xxxxxx10b	Sink test mode declined	00100h : 00106h
xxxxxx11b	Not Legal code	00100h : 00106h

A complete two way AUX transaction is defined as one of the following

1. AUX write and Sink issue ACK reply

From Source						
Sync	Start/Start Pattern	4-bit cmd 1000	20-bit address	8-bit length	Data	Stop

From sink ACK			
Sync	Start bit	00000000	Stop

2. AUX write and Sink issue NACK reply
   For Write transaction:

   A data byte "M" must follow AUX NACK, "M" indicates the number of data bytes successfully written. When a Source Device is writing a DPCD address not supported by the Sink Device, the Sink Device shall reply with AUX NACK and "M" equal to zero.

From Source						
Sync	Start bit	4-bit cmd 1000	20-bit adr	8-bit length	Data	Stop

From sink NACK				
Sync	Start bit	00010000	8-bit data byte M	Stop

3. AUX Read and Sink issue ACK reply
   For Read transaction:

   Ready to reply to Read request with data following.

   DisplayPort receiver may assert a STOP condition before transmitting the total number of requested data bytes when not all the bytes are available.

From Source					
Sync	Start bit	4-bit cmd 1001	20-bit address	8-bit length	Stop

From sink ACK				
Sync	Start bit	00000000	Data	Stop

4. AUX Read and Sink issue NACK reply
   For Read transaction:

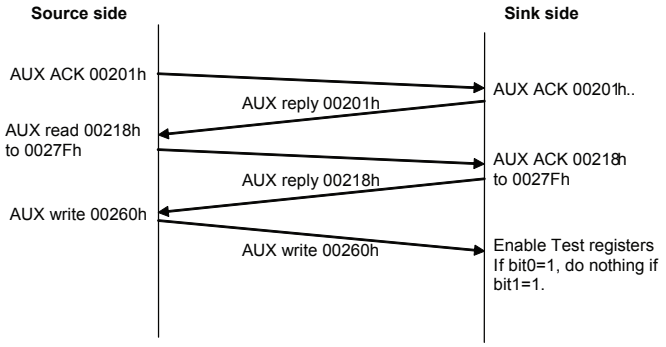
   A Sink Device receiving a Native AUX CH read request for an unsupported DPCD address must reply with an AUX ACK and read data set equal to zero instead of replying with AUX NACK.

From Source					
Sync	Start bit	4-bit cmd 1001	20-bit address	8-bit length	Stop

From Sink NACK				
Sync	Start bit	00001000	data = 0	Stop

Typical AUX Test request handshake sequences with HPD_IRQ

AUX listener stores the last transaction in the register to identify the current transaction type.



Start up Sequence and Hot Plug Detect (HPD) Usage

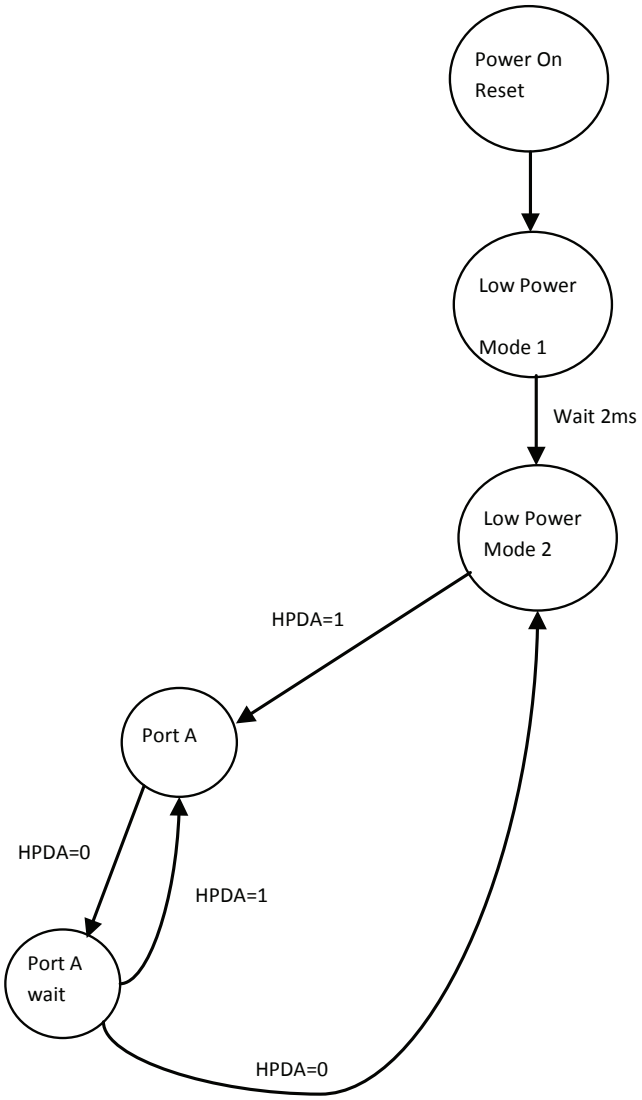
After Power on, HPD_SNK control state machine goes to Low Power state 1 and then state 2, and then monitor HPD_SNK. At Power on Reset state, low power state 1 and low power state 2, all outputs are HiZ, equalizer is powered down, HPD _SRC is HiZ.

At Lower Power Mode State 2, if HPD_SNK is asserted, it will turn output signals active.

If output port is active and HPD_SNK = 0, then it will go to a debounce timer and wait for 300ms, if HPD_SNK is still =0, the controller will return to Low Power mode wait state 2.

If HPD_SNK is 1 then the controller will return to output port active state. HPD_SNK will pass through HPD _SRC.

HPD Detection & Control Circuit State Diagram



Maximum Ratings(1)

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
V3P3 I/O supply voltage to ground potential..... -0.5V to 4.0V
DC Signal Voltage..... -0.5V to V3P3 +0.5V
Current Output .....-25mA to+25mA
Power Dissipation Continous 500mW
Operating Temperature ..... -40 to +85°C
ESD Protection[2]
All Pins, HBM 2kV

Note:

1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) ESD results are for single supply mode only

DC Electrical Characteristics

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V3P3	3.3V Power Supply		3.0	3.3	3.6	V
Control Pin ENABLE						
V_{IH}	LVTTL input high voltage		2.4		V3P3	V
V_{IL}	LVTTL input low voltage		GND		0.8	V
I_{IH}	Input High-level current	V_{IH}=2V to V3P3	-5		5	uA
I_{IL}	Input Low-level current	V_{IL}=GND to 0.8V	-50		-15	uA
HPD_SRC and HPD_SNK Pins						
V_{IH}	LVTTL input high voltage		2.4		V3P3	V
V_{IL}	LVTTL input low voltage		1/3*V3P3		2/3*V3P3	V
I_{IH}	Input High-level current		GND		0.6	uA
I_{IL}	Input Low-level current		20		40	uA
V_{OH}	LVTTL high level output voltage	I_{OH}=-8mA	2.4			V
V_{OL}	LVTTL low level output voltage	I_{OL}= 8mA			0.4	V
AUXP/N, SCL/SDA						
When Configure SCL/SDA pins						
I_{IH}	Input High-level current	VIH=V3P3	-1		1	uA
I_{IL}	Input Low-level current	VIL=0	-1		1	uA
When configure as Aux pins						
Vcom	Common mode voltage		0		2.0	V
V_{AUX-PP}	Peak to peak differential voltage		0.19		1.26	V
R_{ON}	On resistance	Vin = -0.3V to +0.4V ION=-40mA		11	20	Ω
BW	3dB Bandwidth			1		dB

DC Electrical Characteristics

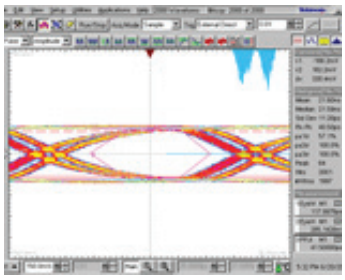
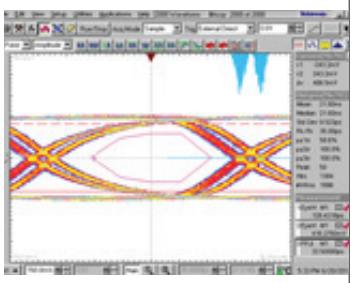
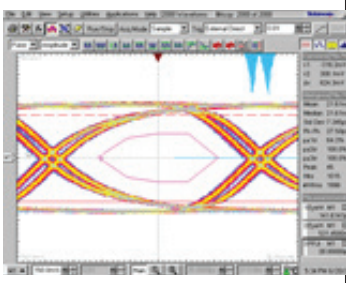
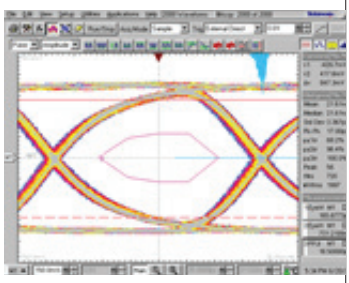
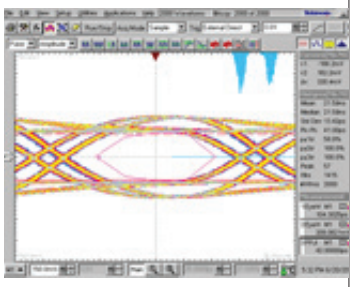
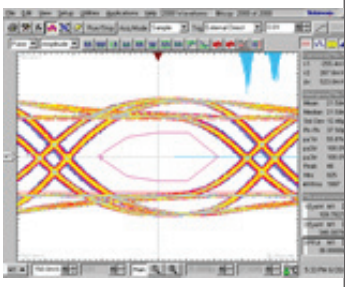
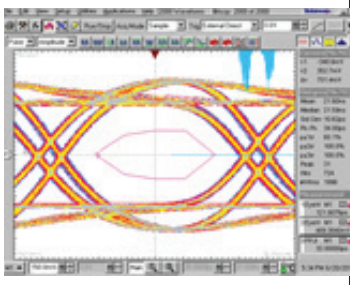
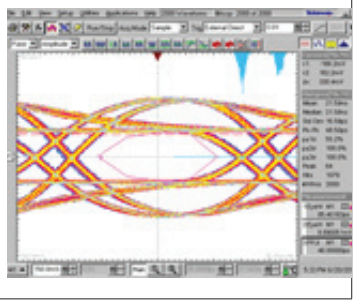
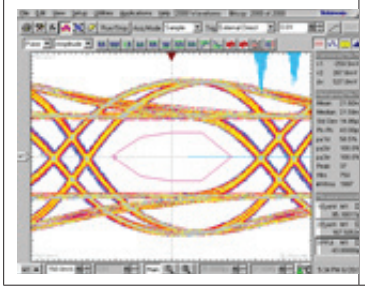
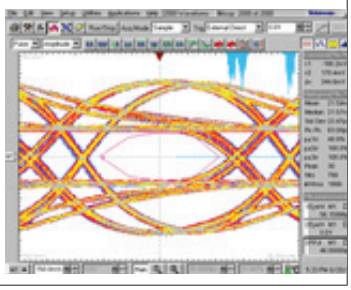
Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
DP differential Input						
V_{ID}	Peak to peak differential input voltage		400		1200	mV
V_{ODO}	Differential overshoot voltage				15%*V3P3	V3P3
V_{ODU}	Differential undershoot voltage				25%*V3P3	V3P3
Ioff	Single end standby current				10	uA
Isc	Output short current				60	mA
DP differential Output						
Vtx diff-lev1	Differential pk-pk level 1		340	400	460	mV
Vtx diff-lev2	Differential pk-pk level 2		510	600	680	mV
Vtx diff-lev3	Differential pk-pk level 3		690	800	920	mV
Vtx diff-lev4	Differential pk-pk level 4		1020	1200	1380	mV
Pre-emphasis level						
0dB	Vtx diff = 0.8V		0	0	0	dB
3.5dB (1.5x)	Vtx diff = 0.8V		2.8	3.5	4.2	dB
6dB (2x)	Vtx diff = 0.8V		4.8	6	7.2	dB
9.5dB (3x)	Vtx diff = 0.8V		7.6	9.5	11.4	dB
DP differential output CML driver AC Switching Characteristics						
Trise / Tfall	Rise and Fall Time	20% to 80 %	80	115	150	ps
Tsk(D)	Intrapair differential skew				50	ps
Tsk(O)	Intrapair differential skew				50	ps

Power Consumption

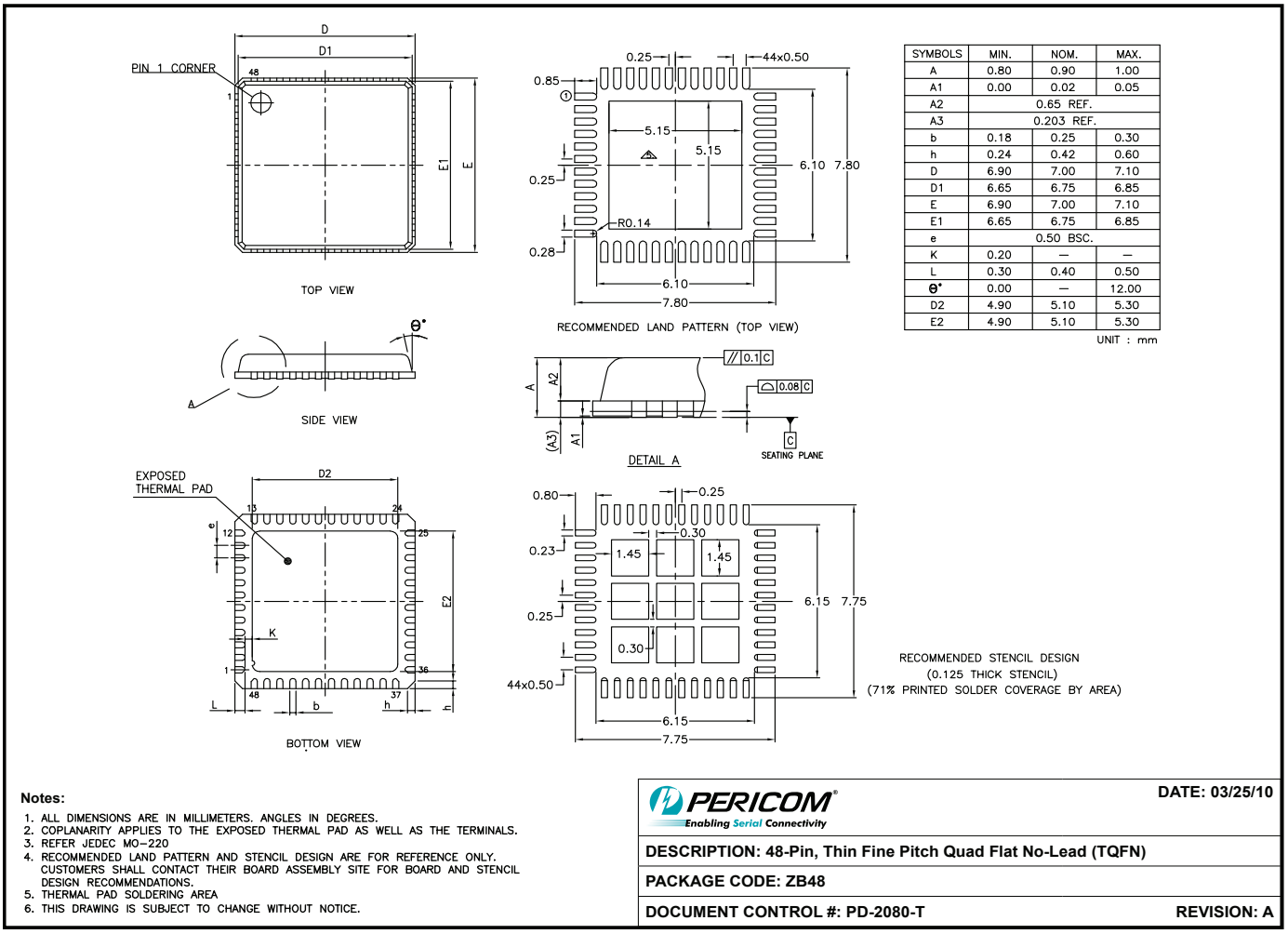
Symbol	Condition		Min	Typ	Max	Units
Icc_V3P3	ENABLE = High, HPD_SNK = High 4 DP lanes active, Pre-emphasis = 0dB, Output Swing = 400mV	5.4Gbps		340		mA
		2.7Gbps		310		
		1.62Gbps		300		
Icc_V3P3_SB	ENABLE = Low			1.4	5	mA
Iccq_V3P3	ENABLE = High, HPD_SNK = Low			4	20	mA
PowerDown_V3P3	AUX Reg 600h = 02h, ENABLE= High, HPD_SNK = High, CNTRL = Low			5		mA

Measured Output Waveforms

As following is shown the actual measured output waveforms on the condition of 5.4Gbps with PRBS27-1 pattern. Auto EQ=High; CAD_Snk=0; HPD=High; OC_1=High; OC_0=OP_0=Low; OP_1=Low; Input Level is 0.6V differential peak-peak with 12-in FR4 Length and 36-in output Coaxial Cable

Swing=400mV, Preemph=0dB	Swing=600mV, Preemph=0dB	Swing=800mV, Preemph=0dB	Swing=1200mV, Preemph=0dB
			
Swing=400mV, Preemph=3.5dB	Swing=600mV, Preemph=3.5dB	Swing=800mV, Preemph=3.5dB	Swing=400mV, Preemphasis=6dB
			
Swing=600mV, Preemph=6dB	Swing=400mV, Preemphasis=9.5dB		
			

Packaging Mechanical: 48-Contact TQFN (ZBE)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.203 REF.	
b	0.18	0.25	0.30
h	0.24	0.42	0.60
D	6.90	7.00	7.10
D1	6.65	6.75	6.85
E	6.90	7.00	7.10
E1	6.65	6.75	6.85
e		0.50 BSC.	
K	0.20	—	—
L	0.30	0.40	0.50
θ°	0.00	—	12.00
D2	4.90	5.10	5.30
E2	4.90	5.10	5.30

Notes:

1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO−220
4. RECOMMENDED LAND PATTERN AND STENCIL DESIGN ARE FOR REFERENCE ONLY. CUSTOMERS SHALL CONTACT THEIR BOARD ASSEMBLY SITE FOR BOARD AND STENCIL DESIGN RECOMMENDATIONS.
5. THERMAL PAD SOLDERING AREA
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

PERICOM® Enabling Serial Connectivity

DATE: 03/25/10

DESCRIPTION: 48-Pin, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZB48

DOCUMENT CONTROL #: PD-2080-T **REVISION: A**

Note: For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Type
PI3EQXDP1201ZBE	ZB	Pb-free & Green, 48-pin TQFN

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

2. E = Pb-free and Green

3. Adding an X suffix = Tape/Reel

Related Products

Part Number	Product Description
PI3HDX1204-B	HDMI2.0 6Gbps ReDriver & Level Shifter
PI3DPX1203	DP1.3 8Gbps ReDriver
PI3HDX511D/E/F	3.4G HDMI1.4 Redriver for Source application, supporting Dual mode DisplayPort
PI3HDX412BD	1:2 Active 3.4Gbps HDMI1.4 compliant Splitter/DeMux/Redriver
PI3HDX414	1:4 Active 3.4Gbps HDMI1.4 compliant Splitter/DeMux/Redriver
PI3HDX621	2:1 3.4Gbps HDMI1.4 Switch/Re-driver with ARC and Fast Switching support for Sink Application
PI3PCIE3242	PCIe 3.0, 1-lane (2-Channel), Differential 2-Lane Exchange (2x2 matrix) switch. 3.3V for Type-C connector
PI3WVR12412	Wide Voltage Range DisplayPort™ & HDMI Video Switch
PI3VDP12412	4-Lane DisplayPort1.2 Compliant Switch

Reference Information

Document	Description
AN	PI3EQXDP1201 Design Guideline for DisplayPort Source Application Note

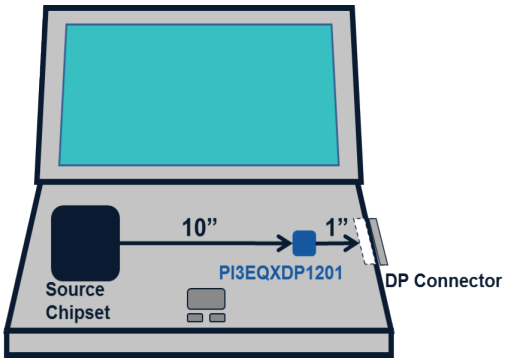
Appendix:

1. Displayport Compliance Test Report

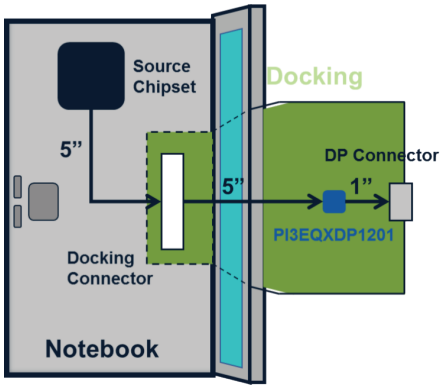
DisplayPort Test Report

Overall Results: 0 of 17 Tests Failed

Test Configuration Details	
Device Description	
Test Specification	1.2
Test Session Details	
Fixture Type	Agilent W2641B
Infiniium SW Version	03.50.0001
Infiniium Model Number	DSO91304A
Infiniium Serial Number	MY51500114
Application SW Version	3.11
Debug Mode Used	No
Last Test Date	9/5/2012 2:12:39 PM



Notebook application example



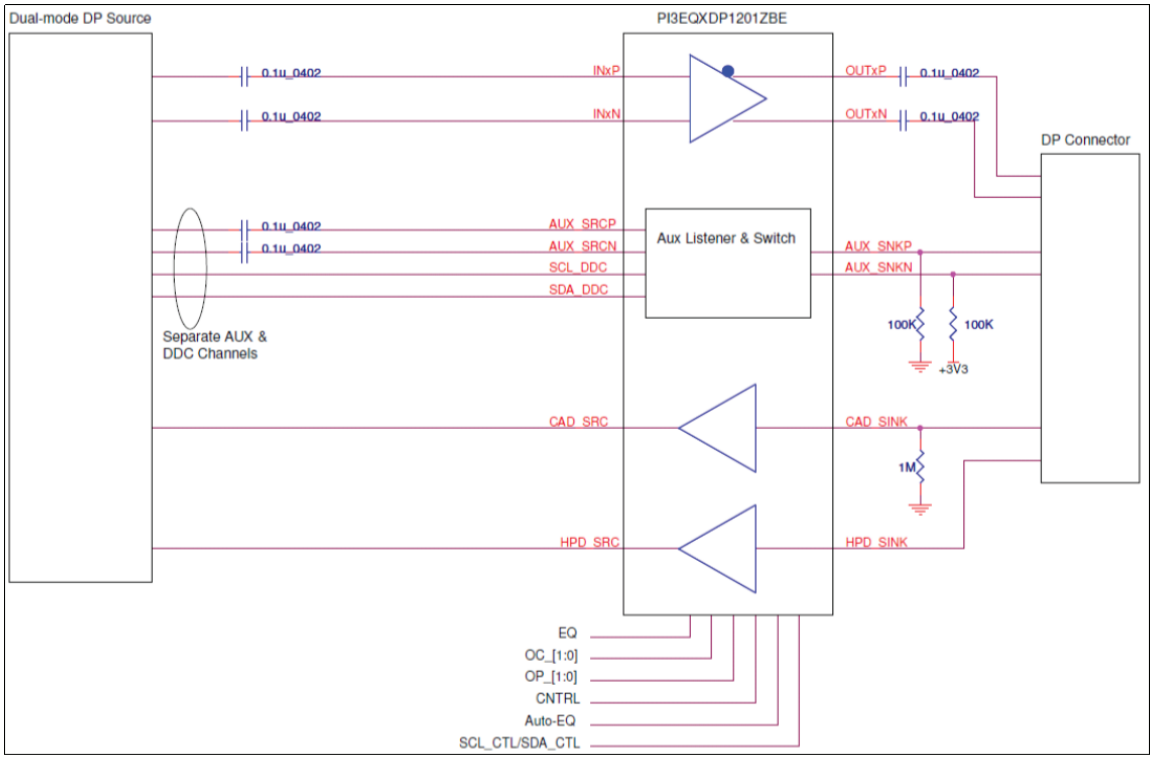
Notebook Docking application example

Summary of Results

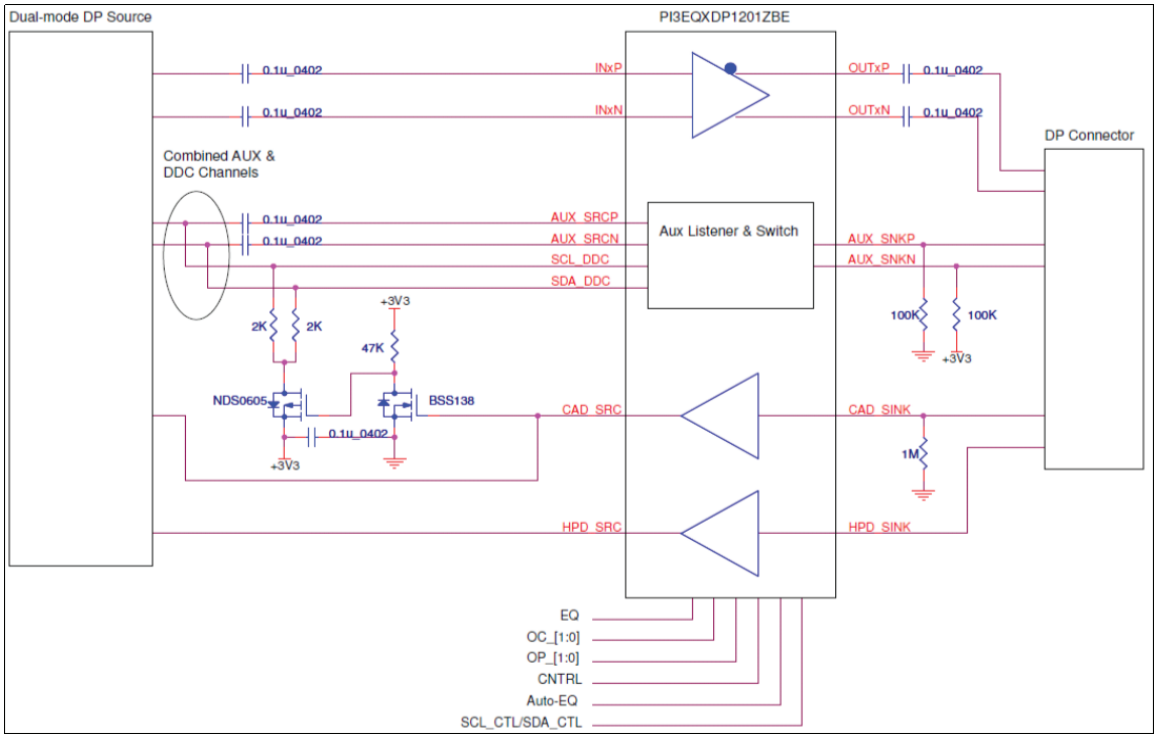
Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Spec Range
✓	0	1	Lane 2 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 0)	5.8709dB	39.5 %	5.2000dB <= VALUE <= 6.9000dB
✓	0	1	Lane 2 - PLTPAT - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	2.4382dB	44.1 %	1.6000dB <= VALUE <= 3.5000dB
✓	0	4	Lane 2 - PLTPAT - Pre-Emphasis Level Test (Pre-emphasis 0)	-862mdB	444.8 %	VALUE <= 250mdB
✓	0	3	Lane 2 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0)	4.277dB	113.9 %	VALUE >= 2.000dB
✓	0	1	Lane 2 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 2)	983m	38.8 %	VALUE >= 708m
✓	0	2	Lane 2 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 2)	2.319dB	44.9 %	VALUE >= 1.600dB
✓	0	1	Lane 2 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 1)	997m	40.8 %	VALUE >= 708m
✓	0	1	Lane 2 - PLTPAT - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 3)	1.675dB	4.7 %	VALUE >= 1.600dB
✓	0	1	Lane 2 - PLTPAT - Non-Transition Voltage Range Measurement (Swing 0)	992m	16.7 %	VALUE >= 850m
✓	0	1	Lane 2 - PLTPAT - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	3.0149dB	40.7 %	1.0000dB <= VALUE <= 4.4000dB
✓	0	1	Lane 2 - HBR2CPAT Eye Diagram Test (TP3_EQ)	0.000	50.0 %	-500m <= VALUE <= 500m
✓	0	1	Lane 2 - HBR2CPAT Total Jitter Test (TP3_EQ)	386.700mUI	33.3 %	VALUE <= 580.000mUI
✓	0	1	Lane 2 - HBR2CPAT Deterministic Jitter Test (TP3_EQ)	268.700mUI	45.2 %	VALUE <= 490.000mUI
✓	0	1	Lane 2 - D10.2 Total Jitter Test (TP3_EQ)	94.500mUI	76.4 %	VALUE <= 400.000mUI
✓	0	1	Lane 2 - D10.2 Deterministic Jitter (TP3_EQ)	11.100mUI	95.6 %	VALUE <= 250.000mUI
✓	0	1	Lane 2 - D10.2 Random Jitter (TP3_EQ)	6.800mUI	97.0 %	VALUE <= 230.000mUI
✓	0	1	Lane 2 - Intra Pair Skew Test	6.34ps	78.9 %	VALUE <= 30.00ps

2. Reference Schematics



Dual-mode DP Source Application Diagram with Separate AUX and DDC Channels from Source



Dual-mode DP Source Application Diagram with Combined AUX and DDC Channels from Source

Revision History

Version	Changes
2015/2/4	Removed 3.3/1.5V power supply and SMBus option for new design. Please contact Pericom if you need this function support.